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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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YOUNG & THOMPSON 745 SOUTH 23RD STREET 2ND FLOOR ARLINGTON, VA 22202			EXAMINER SCIACCA, SCOTT M	
			ART UNIT 2146	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/510,167	Applicant(s) NORDMARK ET AL.	
	Examiner Scott M. Sciacca	Art Unit 2146	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-18 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 04 October 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date ____. | 6) <input type="checkbox"/> Other: ____. |

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1-18 are rejected under 35 U.S.C. 101 because the claimed invention lacks patentable utility. Claims 1-18 do not produce a useful, concrete, and tangible result. The claims broadly mention a method and processing means for processing a packet of data and adding information to or deleting information from the packet. However, the invention as it is claimed does not produce a result that is useful, concrete, and tangible as a result of processing the packet.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-12 and 15-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Sonksen (US 2003/0046429).

Regarding Claim 1, Sonksen teaches a method of pipelined processing of a data packet in a processing means comprising at least two processing stages (*"A method and apparatus for packet processing is disclosed. In one embodiment of the invention the method and apparatus is implemented in plurality of pipeline stages"* – See Abstract), said data packet containing information (*"In most instances, each packet includes a payload portion, containing the data, proceeded by a header portion, containing information about the packet such as the source and destination of the packet, quality of service, packet size and other information"* – See [0002]), said method characterised by associating information reference to said data packet, said information reference comprising information relating to the length and position of the information contained in said data packet (*"Note that in different formats or protocols the entire header may be of different length, items of information may be arranged in different order, pieces of information in the header may be of different length, or additional items of information may be included. Advantageously the dynamic processing module of the invention is able to dynamically adapt and/or accommodate the various different header formats and the challenges presented by different formats"* – See [0081]; In order for the processing module to process packets in different protocols, the order (position) and length of an item of information is associated with the packet); processing said data packet in a processing stage and if said processing of said data packet results in a change of the length or position of said information contained in said data packet, then

altering said information reference in order for said information reference to reflect said change (*"Another aspect of the method and apparatus described herein is the ability to process data as it is passing through a packet processing pipeline to modify or replace packet data, or to change the order of data within the packet, including the header or a tag"* – See [0021]; *"the system may further include a control system configured to determine when the data modifiers modify the data received from the first set of one or more data selectors"* – See [0022]; *"The one or more data modifiers may perform modifications consisting of modification to a time to live value, a type of service value, a checksum value, or other data fields in a packet"* – See [0022]).

Regarding Claim 2, Sonksen teaches adding, prior to the step of associating, at least one bit to said data packet (*"In another method of operation, the invention may comprise a method of adding a tag to a packet comprising identifying a control word to guide processing of a packet and then storing a portion of a packet in a memory"* – [0015]).

Regarding Claim 3, Sonksen teaches the step of adding comprising adding a header and/or a tail to said data packet (*"In another method of operation, the invention may comprise a method of adding a tag to a packet comprising identifying a control word to guide processing of a packet and then storing a portion of a packet in a memory"*).

Regarding Claim 4, Sonksen teaches the method of Claim 1 further comprising the steps of determining, upon the data packet exiting the last of said at least one processing stages, whether any bits of the data packet are superfluous and if any bits of the data packet are superfluous, then removing said superfluous bits (*"It also includes a processing module configured to add supplemental data to a packet or strip data from a packet based on control instructions and the processing location in the packet"* – See [0019]).

Regarding Claim 5, Sonksen teaches the method of Claim 1 further comprising the steps of removing, upon the data packet exiting the last of said at least one processing stages, at least one bit from the data packet (*"It also includes a processing module configured to add supplemental data to a packet or strip data from a packet based on control instructions and the processing location in the packet"* – See [0019]).

Regarding Claim 6, Sonksen teaches said information reference being included in additional information associated with said data packet (*"Note that in different formats or protocols the entire header may be of different length, items of information may be arranged in different order, pieces of information in the header may be of different length, or additional items of information may be included. Advantageously the dynamic processing module of the invention is able to dynamically adapt and/or accommodate the various different header formats and the challenges presented by different formats"* – See [0081]; As shown above with regard to Claim 1, the information reference

(position and length of an information item within a packet) is taken into consideration when the corresponding packet is processed).

Regarding Claim 7, Sonksen teaches the method of Claim 1 wherein prior to said step of processing said data packet, said information reference is stored in at least one register accessible to the processing stage performing said processing (*"The registers discussed herein may comprise one register or a plurality of registers to facilitate clocking in, storage and clocking out of information as required for intended operation of the invention"* – See [0084]).

Regarding Claim 8, Sonksen teaches said information reference comprises a length value and an offset value, said length value representing the length of the information contained in said data packet and said offset value indicating the position in said data packet of the information contained in said data packet (*"Note that in different formats or protocols the entire header may be of different length, items of information may be arranged in different order, pieces of information in the header may be of different length, or additional items of information may be included. Advantageously the dynamic processing module of the invention is able to dynamically adapt and/or accommodate the various different header formats and the challenges presented by different formats"* – See [0081]; In order for the processing module to process packets in different protocols, the length and the location (offset) of an item of information within a packet is associated with the packet).

Regarding Claim 9, Sonksen teaches a processing means for pipelined processing of a data packet (*"FIG. 3 illustrates a block diagram of an example embodiment of a pipeline packet processing system of the invention"* – See [0037]), said processing means comprising at least one processing stage comprising a logic unit (*"Shown in FIG. 3 is a first processing module 312, a second processing module 320 up to an Nth processing module 328"* – See [0062]) and a register for storing at least part of said data packet (*"In one embodiment the input line 300 may carry packets and associated control data to the memory 308 for storage"* – See [0061]), said processing means being characterised in that at least one register for storing information reference associated with said data packet is accessible to said logic unit (*"In operation the data is received on the input 300. It is stored or buffered in some combination in either or both of memory 308 and input buffer 304. To facilitate processing the data is transferred down the pipeline into module 312. Corresponding control store instructions are provided to controller 316 from memory or a memory pointer to the control store in memory is provided to the controller"* – See [0063]); and at least one of at said at least one logic units is adapted to operate upon said information reference (*"The first processing module 312 processes the data in accordance with the controller 316"* – See [0063]).

Regarding Claim 10, Sonksen teaches means for adding at least one bit to said data packet (*"In another method of operation, the invention may comprise a method of*

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adding a tag to a packet comprising identifying a control word to guide processing of a packet and then storing a portion of a packet in a memory” – [0015]).

Regarding Claim 11, Sonksen teaches means for adding comprising a buffer (*“FIG. 8 illustrates an example implementation of one example embodiment of the tag generation module” – See [0043]; “In the embodiment shown in FIG. 8, the FIFO unit 800 includes control word/label storage 804 and packet data storage 806” – See [0083]) and a shifter (*“In the example embodiment shown in FIG. 8, the second register 844 includes four byte shift registers” – [0087]).**

Regarding Claim 12, Sonksen teaches the means of Claim 9 further comprising means for removing at least one bit from said data packet (*“It also includes a processing module configured to add supplemental data to a packet or strip data from a packet based on control instructions and the processing location in the packet” – See [0019]).*

Regarding Claim 15, Sonksen teaches said at least one register for storing information reference being located in said processing stage (Each processing module in Fig. 3 includes an interface to memory 308).

Regarding Claim 16, Sonksen teaches said at least one register for storing information reference comprising one register for storing a length value and another register for storing an offset value (*“In one embodiment the input line 300 may carry*

packets and associated control data to the memory 308 for storage” – See [0061]; “Note that in different formats or protocols the entire header may be of different length, items of information may be arranged in different order, pieces of information in the header may be of different length, or additional items of information may be included.

Advantageously the dynamic processing module of the invention is able to dynamically adapt and/or accommodate the various different header formats and the challenges presented by different formats” – See [0081]; Each data packet stored in memory 308 has position (offset) and length data associated with it).

Regarding Claim 17, Sonksen teaches an integrated circuit characterized by processing means according to Claim 9 (*“In one embodiment an the method and apparatus is enabled in an ASIC-based solution” – See [0012]; The processing means is characterized by an ASIC (application-specific integrated circuit)).*

Regarding Claim 18, Sonksen teaches a computer unit characterized by an integrated circuit according to Claim 9 (*“In one embodiment an the method and apparatus is enabled in an ASIC-based solution” – See [0012]; The processing means is characterized by an ASIC (application-specific integrated circuit)).*

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sonksen (US 2003/0046429) in view of Lee et al. (US 6,996,117).

Regarding Claim 13, Sonksen teaches means for removing comprising a buffer (*"FIG. 17 illustrates an example embodiment of a data modifier system as may be contemplated for use with a pipeline processing system"* – See [0054]; *"Register 1704 has sections A, B, C and D"* – See [0125]), but does not explicitly teach means for removing also comprising a shifter. However, Lee does teach using a shifter as means for removing data (*"The stripped-off information element segment 450 is rotated backward by one place (i.e., shifted to the left by one place) to produce the rotated information element segment 452"* – See Col. 29, lines 65-67). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a shifter as means for removing at least one bit of data. Motivation for doing so would be to implement as much of the processing means as possible in hardware in order to boost performance (See Col. 1, lines 65-67 of Lee's disclosure).

7. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sonksen (US 2003/0046429) in view of Song (US 5,818,894).

Regarding Claim 14, Sonksen teaches means for adding comprising a shifter (See above remarks regarding Claim 11), but does not explicitly teach the shifter being

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a barrel shifter. However Song does teach a barrel shifter with inputs for adding input data (*"A high speed barrel shifter in which fill input data is especially added"* – See Abstract; *"FIG. 1 is a block diagram of an 8-bit barrel shifter according to the present invention"* – See Col. 1, lines 61-62). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a barrel shifter as means for adding at least one bit to a packet of data. Motivation for doing so would be to provide a device which can perform shift operations at high speed while minimizing the necessary logic circuitry (See Col. 1, lines 25-27 of Song's disclosure).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Scott M. Sciacca whose telephone number is (571) 270-1919. The examiner can normally be reached on Monday thru Friday, 7:30 A.M. - 5:00 P.M. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeff Pwu can be reached on (571) 272-6798. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS



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SUPERVISORY PATENT EXAMINER